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Low-Power 1-bit CMOS Full Adder Using Subthreshold Conduction Region

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Abstract— In balancing the trade-off between power, area and performance, numerous efforts have been done. However, not much study has been done at the two extreme ends of the design spectrum, namely the ultra low-power with acceptable performance at one end (the main concern of this paper), and high performance with power within limit at the other. This paper is based on the exclusive use of subthreshold conduction currents to perform circuit operations, yielding a dramatic improvement in power consumption compared to traditional circuit design approaches. This improvement makes it feasible to design extreme low-power circuits with such an approach. The CMOS digital circuits for this work have been designed using standard TSMC 0.18 *μm* Technology.

Index Terms— Low-Power, Subthreshold Conduction Region, Full Adder.
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1 INTRODUCTION

IN most VLSI applications, arithmetic operations play an important role. Commonly used operations are addition, subtraction, multiplication and accumulation, and 1-bit Full Adder is the building block for most implementations of these operations. Obviously, enhancing the building block performance is critical for enhancing overall system performance [1] and in present, the power consumption has become a critical concern in today's VLSI system design. The need for low-power VLSI systems arises from two main forces. First, with the steady growth of processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low-power design directly leads to prolonged operation time in these portable devices [2].

Subthreshold circuit design provides an efficient solution to significantly reduce the power. So this work is based on subthreshold conduction principle to design a low-power 1-bit Full Adder. In subthreshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor. Due to the quadratic reduction in power with respect to the supply voltage, subthreshold circuits are classified as *ultra low-power circuits*.

Specifically in application areas where performance can be sacrificed for low-power, subthreshold circuits are an ideal fit. Some of the applications include devices such as digital wrist watches, radio frequency identification (RFID), sensor nodes, pacemakers and battery operated devices such as, cellular phones [3].

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2 MOTIVATION OF POWER REDUCTION

Up until now, the power consumption has not been of great concern because of the availability of large packages and other cooling techniques having the capability of dissipating the generated heat. However, continuously increasing density as well as the size of the chips and systems might cause to difficulty in providing adequate cooling and hence, might either add significant cost to the system or provide a limit on the amount of the functionality that can be provided [4].

Another factor that fuels the need for low-power chips is the increased market demand for portable consumer electronics powered by batteries. For these high performance portable digital systems, running on batteries such as-laptops, cellular phones and personal digital assistants (PDAs), low-power consumption is a prime concern because it directly affects the performance by having effects on battery longevity.

Hence, low-power 1-bit Full Adder design has assumed great importance as an active and rapidly developing application in VLSI. Due to their extreme low-power consumption, subthrehsold design approaches are appealing for a widening class of applications which demand low-power consumption and can tolerate larger circuit delays.

3 SUBTHRESHOLD CONDUCTION FOR LOW-POWER VLSI DESIGN

Digital subthreshold circuits are currently used for some low-power applications such as hearing aids, wrist watches, pacemaker and wireless communication systems [5]. In subthreshold circuit design, supply voltage must be scaled down below the threshold voltage. Therefore, the load capacitance is charged or discharged by the subthreshold leakage current. When the Adder circuits operate in the subthreshold region, they should have different performance characteristics than those of the Adders working in the strong inversion region [6]. In this paper, we will see the characteristics of a 1-bit Full Adder cell operating in subthreshold region of operation comparing it with the 1-bit Full Adder cell operating in strong inversion.

In traditional digital VLSI design, subthreshold region of operation is avoided, since it contributes toward leakage power consumption when the device is in stand-by. But the power can be reduced significantly by exclusively utilizing this subthreshold leakage current to implement circuits. This is achieved by actually setting the circuit power supply V_{dd} to a value less than or equal to V_{th}. The subthreshold current is exponentially related to gate voltage giving the exponential reduction in power consumption, but also an increase in circuit delay [7]. So, we use the circuits operating in subthreshold conduction region where the power is main concern and large delay can be tolerated.

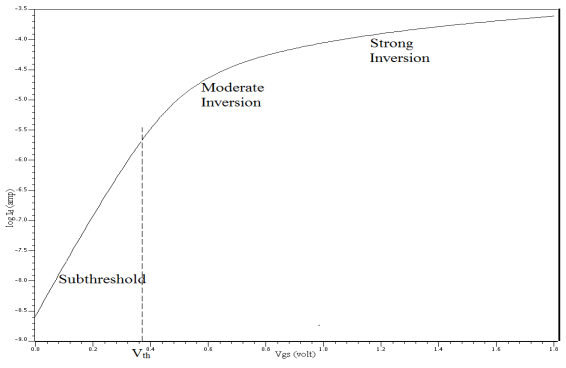

Fig. 1 CMOS Conduction region for an NMOS with V_{ds}= 1.8 V and V_{gs}varying from 0 V to 1.8 V.

Unlike moderate and strong inversion, in which the drift component of current dominates, subthreshold conduction is dominated by diffusion current [8].

3.1 **Modelling of Subthreshold Current**

In subthreshold conduction, the channel of the transistors is not inverted and current flows by diffusion. Subthreshold current can be expressed by the following basic equation:

$$I_{on-sub} = I_0 \, exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right) \quad (1)$$

Equation (2) shows the same basic equation with low V_{ds} roll-off:

$$I_{on-sub} = I_0 \, exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (2)$$

where I_0 is the drain current when V_{gs}= V_{th} given below:

$$I_0 = \mu_{eff} C_{ox} \frac{W}{L_{eff}} (n-1) V_T^2 \quad (3)$$

As expected for the diffusion current, (1) shows that I_{on-sub} depends exponentially on V_{gs}. Here, W is the width of the transistor, L_{eff} is the effective length, μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, n is the subthreshold slope factor $\left(n = 1 + \frac{C_d}{C_{ox}}\right)$, V_{th} is the transistor threshold voltage and V_T is the thermal voltage, $V_T = (kT/q)$.

4 Minimum Energy Point Model

In this section, we will discuss a closed form solution for the optimum V_{dd} and V_{th} for a given frequency and technology operating in the subthreshold region means (V_{dd} V_{th}).

The total energy per operation of a digital CMOS circuit consists of two components: switching and leakage energy [9]. Here, we discuss in terms of an inverter.

Hence, total energy per operation can be expressed as:

$$E_{Total} = E_{SW} + E_L$$

$$= V_{dd}^2 \left(C_{eff} + W_{eff} K C_g L_{DP} exp\left(\frac{-V_{dd}}{nV_T}\right)\right) \quad (4)$$

where, C_{eff} is the average effective switched capacitance per operation, K is a delay fitting parameter, C_g is the output capacitance of the inverter and L_{DP} is the depth of the critical path.

By using (1), (2), (3) and (4), the equations for optimum supply voltage $V_{dd,opt}$ and optimum threshold voltage $V_{th,opt}$ can be derived as shown in (5) and (6) respectively [3].

$$V_{dd,opt} = nV_T \left(2 - \text{lambert W}\left(\frac{-2C_{eff}}{W_{eff} K C_g L_{DP}} exp(2)\right)\right) \quad (5)$$

Also, we can find the optimum value of $V_{th} = V_{th,opt}$ for a given frequency f as:

$$V_{th,opt} = V_{dd,opt} - nV_T \, log_e\left(\frac{f K C_g L_{DP} V_{dd,opt}}{I_0}\right) \quad (6)$$

If the argument to the natural log in (6) exceeds 1, then the assumption of subthreshold operation no longer holds because $V_{th,opt}$ $V_{dd,opt}$. This constraint shows that there is a maximum achievable frequency for a given circuit in the subthreshold region [9].

Swanson and Meindl analysed the VTC of an inverter

and showed that the inverter operation could be simulated down to 100 mV [10]. The VTC curves for different supply voltages for an inverter are shown in Fig. 2. To find the minimum voltage, Swanson equated the *off* current of NMOS and PMOS and calculated the inverter gain in subthreshold. Since an inverter must have sufficient gain at $V_{dd}/2$, the minimum voltage to be used was estimated to be 8(*kT*/*q*) or 0.2 V [10].

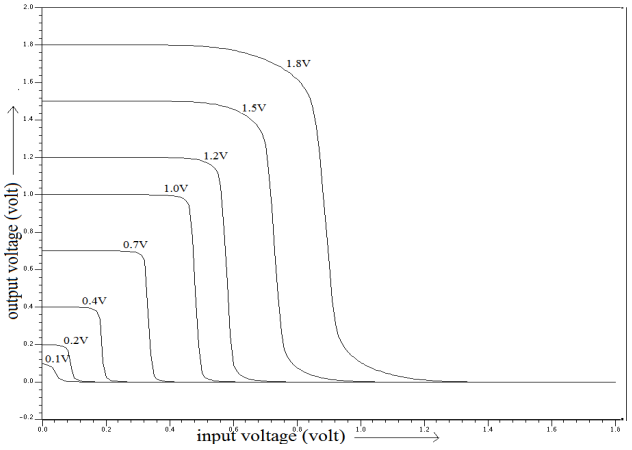

Fig. 2 Inverter VTC showing operation down to 100 mV in a 0.18 *µm* process.

5 Designing Of Low-Power 1-Bit CMOS Full Adder

This section describes the design of 1-bit CMOS Full Adder operating in subthreshold conduction region. Before this design, the basic CMOS Inverter, shown in Fig. 3, is analysed in detail and then, based on this analysis, 1-bit Full Adder can be designed by calculating the values of *W*/*L* with the help of these *W*/*L* values of Inverter which has been designed for symmetric output and equal charging and discharging current.

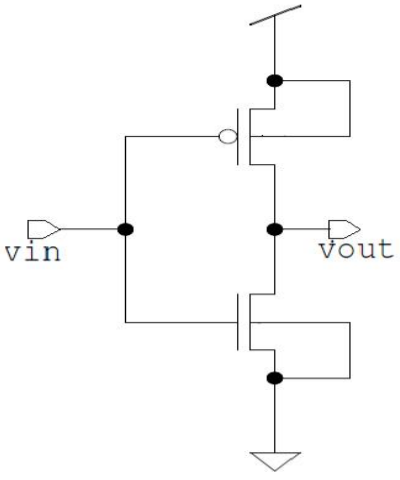

Fig. 3 Basic CMOS Inverter

By simulating this CMOS Inverter using TSMC 0.18 *µm* technology, the Inverter's values of *W*/*L* for PMOS = (1.2 *µm*/0.18 *µm*) and *W*/*L* for NMOS = (0.27 *µm*/0.18 *µm*) were obtained for strong inversion operation. While the Inverter's values of *W*/*L* for PMOS = (3.0 *µm* /0.18 *µm*) and *W*/*L* for NMOS = (0.27 *µm*/0.18 *µm*) were obtained for subthreshold operation.

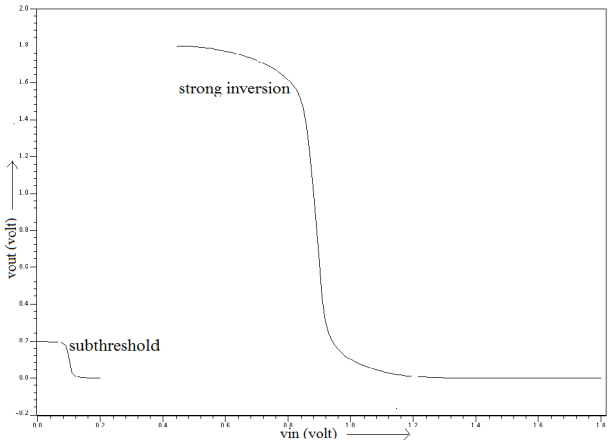

Fig. 4 VTC curves for Inverters operating in strong inversion and subthreshold.

Using these values of *W*/*L* of basic Inverter, Full Adder circuit can be designed having the equivalent *W*/*L* values equal to that of this basic Inverter [3].

6 Design and Simulation Results

6.1 CMOS Inverter

The load capacitance, for the inverter described in previous section, for strong inversion region is 5 *fF* while the load capacitance for subthreshold conduction is 11 *fF*.

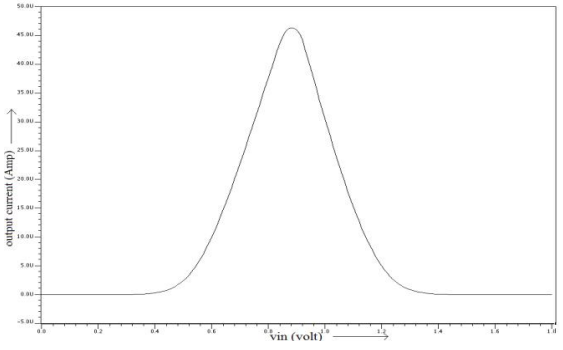

Fig. 5 Output current variation with input voltage in strong inversion region with V_{dd} = 1.8 V.

From Fig. 5 and 6, it is clear that the current depends on input (gate) voltage linearly in strong inversion region and exponentially in subthreshold region.

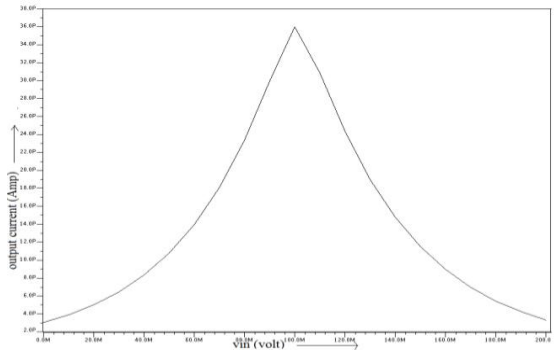

Fig. 6 Output current variation with input voltage in subthreshold region with V_{dd} = 0.2 V.

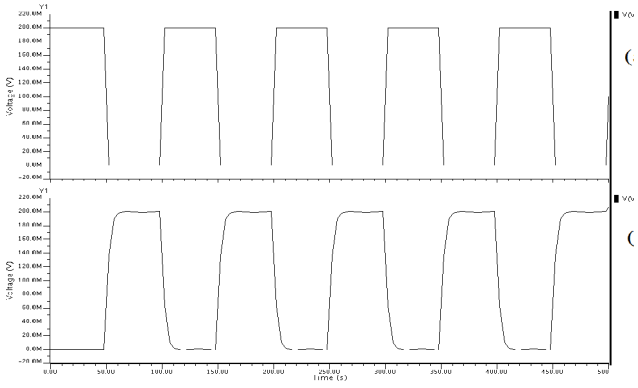

Fig. 7 Simulation result of transient analysis for CMOS Inverter in subthreshold region: (a) Input Signal, (b) Voltage waveform of Output Signal.

Fig. 8 shows the dynamic power variation with different clock frequencies for a 1-bit Full Adder operating in subthreshold conduction region.

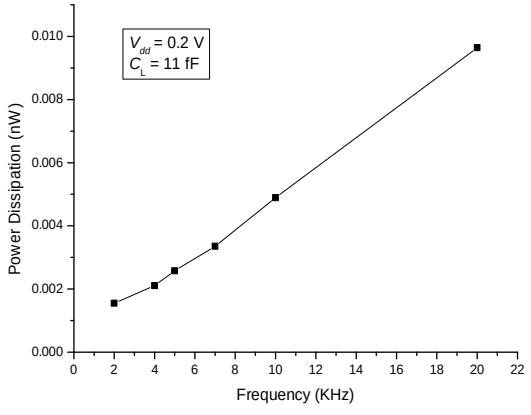

Fig. 8 Power dissipation results for a CMOS Inverter operating in subthreshold conduction region.

6.2 **1-Bit CMOS Full Adder**

A Full Adder is basic structure for any arithmetic circuit, so the design of a Full Adder is very necessary. The basic structure and simulation result for a 1-Bit CMOS Full Adder are shown in figures given below.

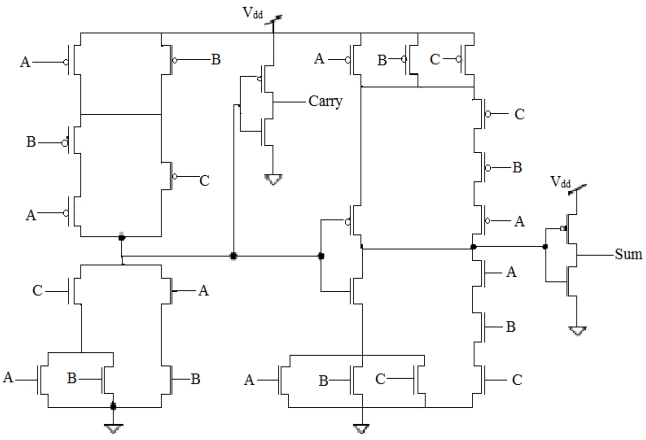

Fig. 9 Basic Structure of a 1-Bit CMOS Full Adder.

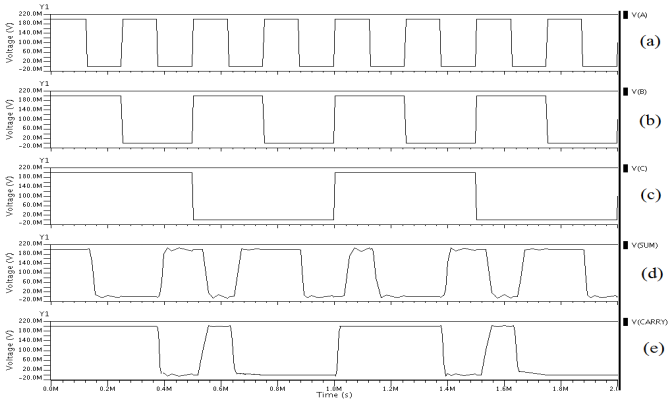

Fig. 10 Simulation result of transient analysis for a 1-Bit CMOS Full Adder in subthreshold conduction region: (a) Input Signal (A), (b) Input Signal (B), (c) Input Signal (C), (d) Voltage waveform of Output (SUM) Signal, (e) Voltage waveform of Output (CARRY) Signal.

TABLE I
POWER DISSIPATION RESULTS

	Operating Frequency (kHz)	Power (nW)	
		Superthreshold region	Subthreshold region
CMOS Inverter	2 k	275.87 n	0.00156 n
	4 k	389.54 n	0.00211 n
	5 k	486.93 n	0.00258 n
1-bit Full Adder	2 k	535.54 n	0.01652 n
	4 k	971.15 n	0.02441 n
	5 k	1100.94 n	0.02793 n

Fig. 11 shows the dynamic power variation with different clock frequencies for a 1-bit Full Adder operating in subthreshold conduction region.

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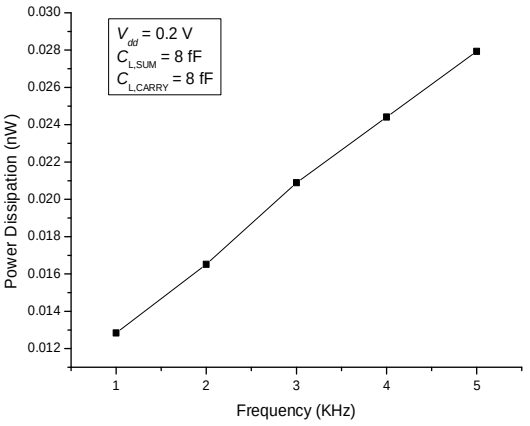

Fig. 11 Power dissipation results for a 1-bit CMOS Full Adder operating in subthreshold conduction region.

7 Layout Designs And Post-Layout Simulation Results

After completing the physical layout design of all the structures, they are matched with schematics using layout versus schematic (LVS) simulation. LVS is done to determine whether a particular layout design corresponds to the original schematic of circuit diagram of the design.

7.1 CMOS Inverter

For a CMOS Inverter operating in subthreshold conduction region, layout and post-layout simulation results are shown in Fig. 12, 13 and 14 respectively.

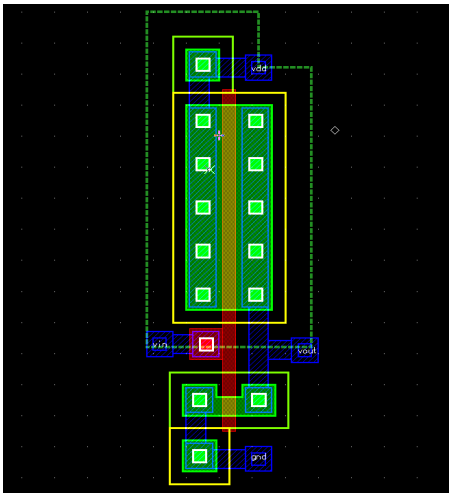

Fig. 12 Layout of CMOS Inverter operating in Subthreshold conduction region.

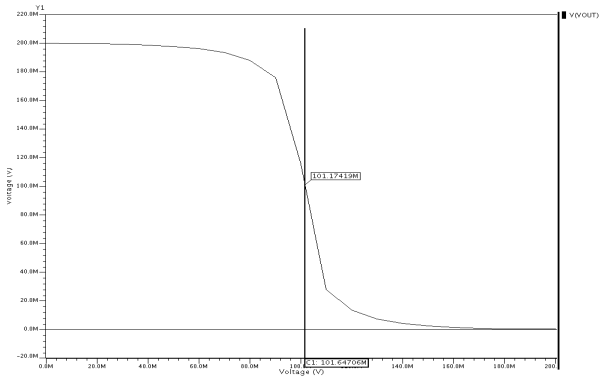

Fig. 13 Post-Layout Simulation – VTC curve for CMOS Inverter operating in subthreshold conduction region.

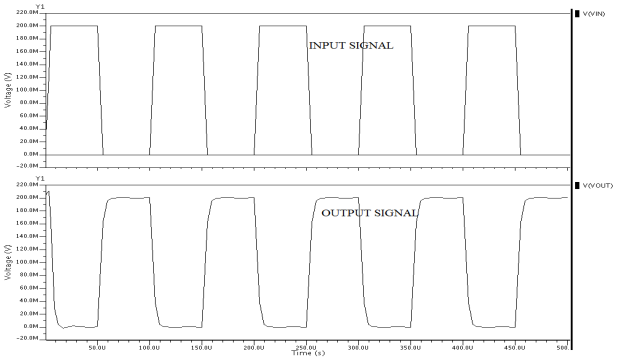

Fig. 14 Post-Layout Simulation – Transient analysis for CMOS Inverter operating in subthreshold conduction region.

7.2 1-Bit CMOS Full Adder

For a 1-bit CMOS Full Adder operating in subthreshold conduction region, layout and post-layout simulation results are shown in Fig. 15 and 16 respectively.

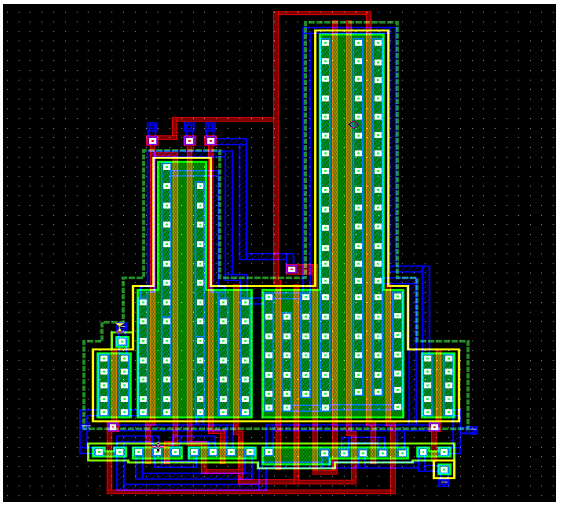

Fig. 15 Layout of 1-bit CMOS Full Adder operating in subthreshold conduction region.

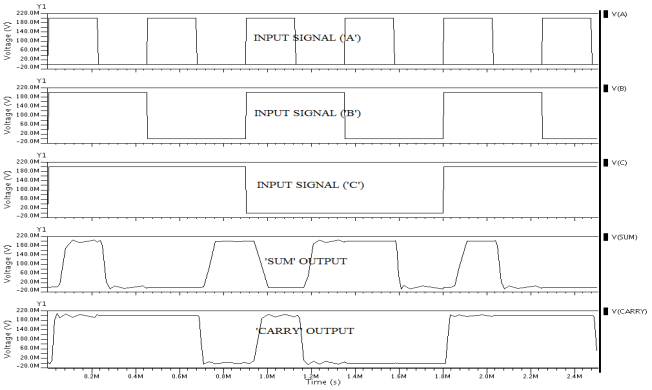

Fig. 16 Post-Layout Simulation – Transient analysis for 1-bit CMOS Full Adder operating in subthreshold conduction region.

8 CONCLUSIONS

Based on the subthreshold conduction region, the designing of a 1-bit CMOS Full Adder has been done. The supply voltage used for the circuits operating in subthreshold conduction region is 0.2 V. The power analysis has also been carried out for the circuits operating in subthreshold conduction region and in strong inversion region. It is found that the circuits operating in subthreshold conduction region provide the significant power reduction than the strong inversion region.

Also, it can be found that subthreshold conduction region is advantageous in applications where power is the main concern and performance can be sacrificed to achieve the low-power because the speed of a circuit operating in subthreshold conduction region becomes significantly slow.

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